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HEADQUARTERS OPERATIONS
MITEL SEMICONDUCTOR
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

MITEL SEMICONDUCTOR
1500 Green Hills Road,
Scotts Valley, California 95066-4922
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576/6231

Internet: http://www.gpsemi.com
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- **UK, EIRE, DENMARK, FINLAND & NORWAY**
  Swindon Tel: (01793) 726666 Fax : (01793) 518582

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APPENDIX 3 (2ND ORDER TYPE 2 SYSTEM)

System Transfer Characteristics

$$G(s) = \frac{\frac{PN}{M}\left[1 + 2\,\underline{s}\right]}{\underline{s}^2 + 2\,\zeta\,\underline{s} + 1}$$

Where:-
Normalised Laplace variable is

$\underline{s} = s/\omega_o$
Natural Frequency is
$\omega_o = \sqrt{\frac{K_d K_o}{PN T_1}}$
Damping Factor is
$\zeta = \omega_o T_2/2$

$T_1 = C_1$

$T_2 = \left[1 + \frac{C_2}{C_1}\right] R_1 C_1$

Open Loop Gain

$$G_{OL}(s) = \frac{1 + 2\zeta\,\underline{s}}{\underline{s}^2}$$

Open Loop Frequency Responses

amplitude

$$A_{OL}(\omega) = \frac{\sqrt{1 + 2\zeta\,\underline{\omega}^2}}{\underline{\omega}^2} \qquad \text{Where } \underline{\omega} = \frac{\omega}{\omega_0}$$

phase
$\varnothing_{OL}(\omega) = - \quad + \text{atan}(2\zeta\omega)$

Phase Margin

$\varnothing_1 = \text{atan}(2\zeta\underline{\omega})$
where unity gain frequency $\omega_1 = \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}$
$\therefore \zeta = \frac{\tan\varnothing_1}{2\,(1 + \tan\varnothing_1)}$

System Frequency Response (See Figure 11)

Amplitude, Phase

$$A(\omega) = \frac{\sqrt{1 + (2\zeta\underline{\omega})^2}}{\sqrt{(1 - \underline{\omega}^2) + (\zeta\underline{\omega})^2}}, \quad \varnothing(\omega) = \text{atan}(2\zeta\underline{\omega}) - \text{atan}\left(\frac{\zeta\underline{\omega}}{1 - \underline{\omega}^2}\right)$$

Time Domain Response (See Figure 12)

$$\omega_{out}(t) = \omega_{out}\left[1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1 - \zeta^2}}\left(\cos\sqrt{1 - \zeta^2}\,\omega_n - \frac{\zeta}{\sqrt{1 - \zeta^2}}\sin\sqrt{1 - \zeta}\,\omega_n\right)\right]$$

$\omega_{out}(t)$ = output frequency at time t.
ω_{out} = output frequency step caused by reprogramming the divider

Settling Time

$$ts = \frac{-\,\text{Ln}\left[\frac{\omega_e}{\omega_{out}}\sqrt{1 - \zeta^2}\right]}{\omega n \zeta}$$

Where $\omega_e = \omega_{out} - \omega_{out}(ts)$ radians/sec
is the error in the output frequency at time ts following a step adjustment of the output frequency of ω.

USE OF VARACTOR LINE DISABLE (OS BIT) IN TUNER ALIGNMENT

In tuner manufacture, many of the wound components must be aligned to give the desired tilt factors, filter matching and correcting range for local oscillators and IF output.

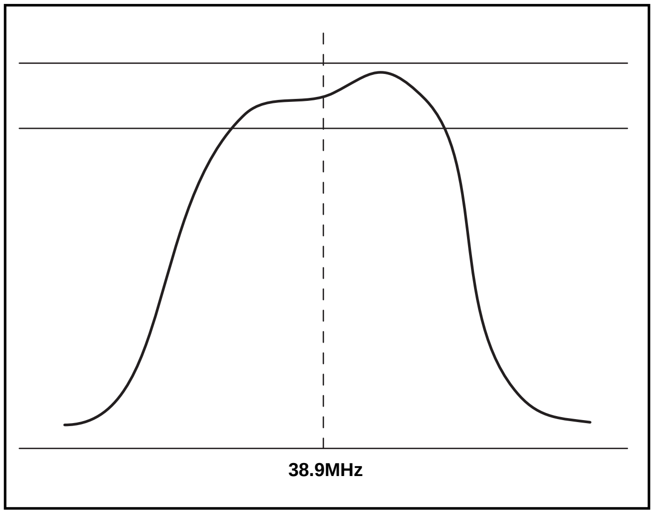


Fig.16 Alignment of IF output

This is a time-consuming process and is usually carried out by tuning the synthesiser to a number of different channels and aligning to these points (shown ● on Fig.17).

Each time a new channel is selected, data must first be written to the synthesiser. In this example, 6 sets of data must be sent from the micro to the synthesiser.

However, if the varactor line disable bit OS is used, the varactor line voltage can be externally controlled. This allows the selected channels to be tuned without the use of a micro to address and program the device.

The varactor line disable facility is available on all Mitel I^2C bus synthesisers and also on I^2C bus compatible 3-wire synthesisers such as the SP5024 and SP5054. With the latter devices, the varactor drive is disabled by applying a negative voltage to the ENABLE pin (pin 10) and sourcing greater than 350µA from the device. using this method of tuning can result in appreciable saving of test time.

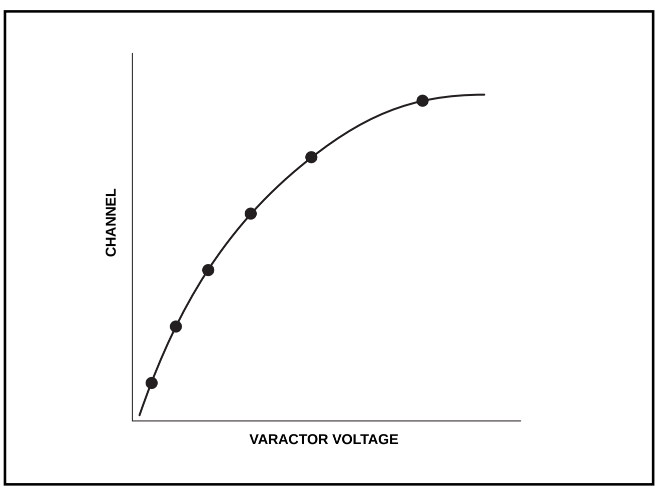


Fig.17 Varactor tuning curve

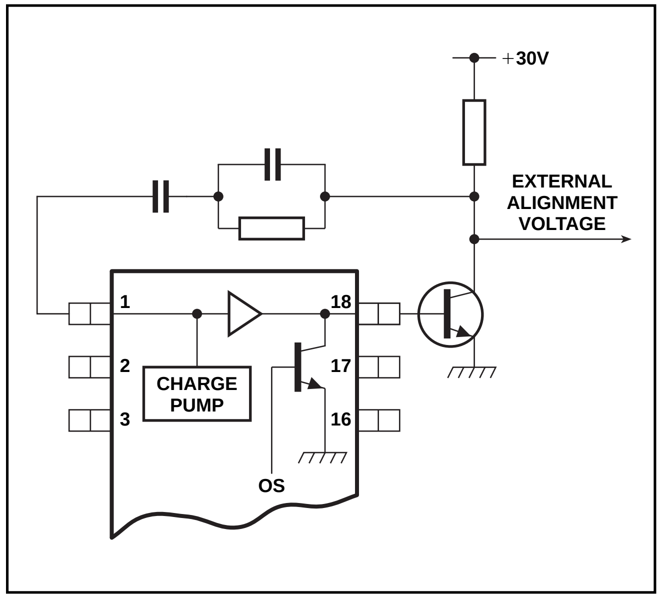


Fig.18 Application of external tuning voltage

APPENDIX 1 (NOTATION)

Description of symbols used.

$\theta_{out}(s)$	=	VCO output phase
$\theta_{in}(s)$	=	Reference oscillator phase
$\omega_{out}(s)$	=	VCO output frequency
$\omega_{in}(s)$	=	Reference oscillator frequency
K_O	=	VCO gain in rads/sec/volt
K_d	=	Phase detector gain = $\frac{Icp}{2}$ Amps/rad
M	=	Reference divider ratio
P	=	Prescaler divider ratio
N	=	Programmable divider ratio
ω_O	=	Natural frequency of 2nd order system in rads/sec
ζ	=	Damping factor of 2nd order system
S	=	Laplace frequency variable
$\underline{S}$	=	S/ω_O = Normalised laplace frequency variable
$\underline{\omega}$	=	ω/ω_O = Normalised frequency

APPENDIX 2 (SYSTEM EQUATIONS)

System Transfer Characteristics (See Figure 9)

$$G(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{K_O K_d (s) / Ms}{1 + K_O K_d (s) / PNs}$$

Open Loop Gain

$$G_{OL}(s) = K_o K_d F(s) / PNs$$

In practice, since the phase detector noise floor predominates, the reference oscillator noise may be ignored. If the phase detector noise floor is -130 dBc then the noise floor at the output is given by :-

θ_{out} = -130dBc + 20 log 65536 = -130 + 96.3 = -33.7dBC

Example (High Comparison Frequency Synthesiser)

The SP5058 has been designed to operate, with a high comparison frequency, typically 250 KHz. If an LO of 2.048 GHz is to be synthesised then :-

$$PN = \frac{2.048 \times 10^9}{250 \times 10^3} = 8192$$

If the phase detector noise floor is -140 dBc then the noise floor of the output is :-

θ_{out} = -140dBc + 20 log 8192 = -140 + 78.3 = -61.7dBC

High comparison frequency synthesisers are used in applications where the phase noise within the loop bandwidth is an important consideration such as scrambled satellite or cable systems using the double conversion principle. See Figure 15 (shown below).

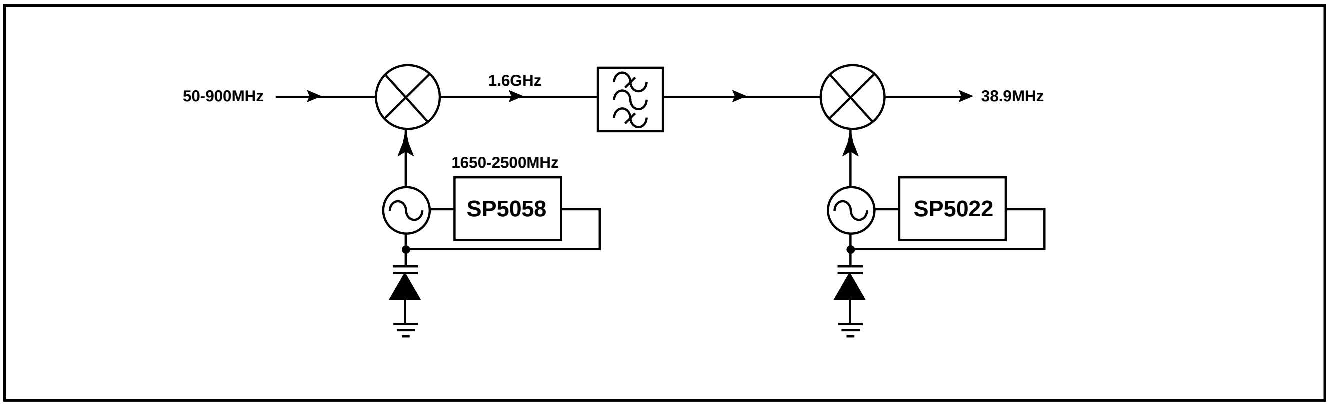


Fig.15 Example of double conversion from VHF/UHF frequencies to TV IF

PHASE NOISE CONSIDERATIONS

Noise Sources (See Figure 12)

The noise present at the VCO output originates from three main sources.

(a) Phase noise in the reference oscillator θ_r
(b) Phase noise in the detector θ_d
(c) Phase noise in the VCO θ_O.

A small sinusoidal frequency modulation of the reference oscillator for example, with peak phase deviation of θ_r radius and modulation frequency ω_m would produce an output voltage of :-

$$V_r(t) = V\cos(\omega_r t+\theta_r \sin\omega_m t)$$
$$= V\cos(\omega_r t) - \frac{V\theta_r}{2}\cos[(\omega_r+\omega_m)t] - \frac{V\theta_r}{2}\cos[(\omega_r-\omega_m)t]$$

See Figure 13. Many such sidebands will be contributed by random noise modulation mechanisms in the reference oscillator such as thermal and schott noise.

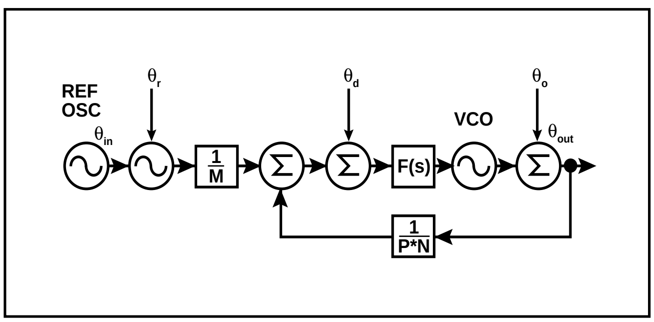


Fig.12 System diagram including phase noise

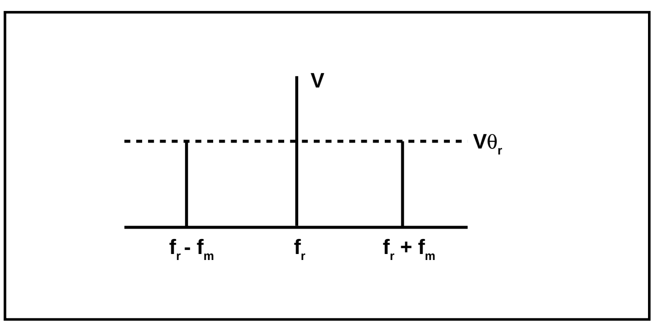


Fig.13 Noise sidebands

Noise at Synthesiser Output

The analysis of the System block diagram shows that the output noise spectrum is determined by :-

$$\theta_{out}(\omega) = A(\omega)\,\theta_r(\omega) + MA(\omega)\,\theta_d(\omega) + \left[1 - \frac{MA(\omega)}{PN}\right]\theta_O(\omega)$$

Where $A(\omega)$ is the system frequency response, described in Appendix 3 (system transfer charateristics) and shown in Figure 10.

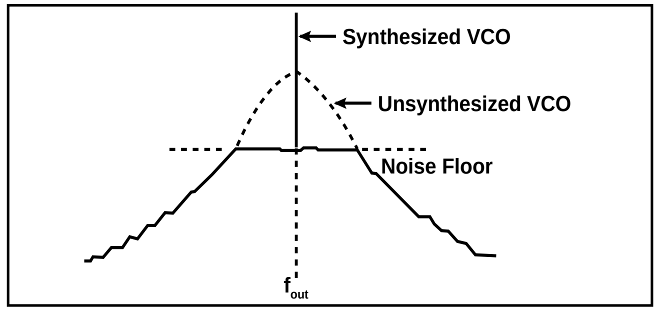


Fig.14 Output spectrum

Noise inside the Loop Bandwidth

The system frequency response inside the loop bandwidth is approximately given by :-

$$A(\omega) = \frac{PN}{M}$$

$\frac{PN}{M}$ This is just a statement that the system output frequency is $\frac{PN}{M}$ times bigger than the reference frequency. As a result the noise at the output is :-

$$\theta_{out\,INBAND}(\omega) = \frac{PN}{M}\theta_r(\omega) + PN\,\theta_d(\omega)$$

Notice that the phase noise due to the phase detector is M times bigger than the phase noise from the reference oscillator. Thus the phase detector noise dominates. This noise appears as a plateau on the spectrum analyser display as shown in Figure 14. The inband VCO noise meanwhile has been suppressed by the loop filter. Thus the inband output noise is determined by the prescaler and programmable divider ratios and by the noise floor of the detector.

$$\theta_{outINBAND} = PN\,\theta_d(\omega)$$

Noise outside the Loop Bandwidth

The output noise outside the loop bandwidth is approximately given by :-

$$\theta_{outOUTBAND} = \theta_O(\omega)$$

This shows that any noise components due to the VCO having frequencies outside the loop bandwidth are <u>not</u> suppressed. Thus the phase noise outside of the loop bandwidth is determined largely by the performance of the VCO itself and no improvement of this can be gained by the use of the synthesiser. See Figure 14.

Example (Low Comparison Frequency Synthesiser)

A synthesiser such as the SP5510 operates with a comparison frequency of 7.8125 KHz. If an LO of 512 MHz is to be synthesised then :-

$$PN = \frac{512 \times 10^6}{7.8125 \times 10^3} = 65536$$

Example (Selection of ω_o and ζ)

Assume the reprogramming causes a frequency step of 512 MHz and we wish the VCO to settle to an accuracy of 5.12 Hz within 100 mS. If the phase margin is 70° then the values for ζ and ω_O are:-

$$\zeta = \frac{\tan Ø}{2\ (1+\tan^2 Ø)} = \frac{\tan 70°}{2\ (1+\tan^2 70°)} = 0.8$$

$$\omega_n = \frac{-\mathrm{Ln}\left[\frac{\omega_e}{\omega_{out}}\sqrt{1-\zeta^2}\right]}{\zeta\, ts} = \frac{-\mathrm{Ln}\left[\frac{5.12}{512x10^6}\sqrt{1-0.8^2}\right]}{0.8 \times 0.1}$$

$\therefore \omega_n =$ 237 rads/sec = 37Hz

Design Formulae

Using the known values of ω_o and ζ we have :-

$$C_1 = \frac{KdKo}{PN\omega_o^2}$$

$$R_2 = \frac{2\zeta}{\omega_o C_1}$$

$$C_2 = C_1/5$$

Example (Selections of C_1, C_2 and R_2)

Suppose Kd = 150µA/2 µA/rad y, K_O = 20 MHz/volt, P = 8, N = 10,722 whilst ω_O = 440 rads/sec and ζ = 0.87.

$$\therefore\ C1 = \frac{150 \times 10^{-6} \times 20 \times 10^6 \times 2}{8 \times 10722 \times 440^2 \times 2} = 180.16\text{nF}$$

$$R2 = \frac{2 \times 0.87}{440 \times 180.6 \times 10^{-9}} = 21.9\text{K}$$

$$C2 = C_1/5 = 36.12\text{nF}$$

ω_O = 440 rads/sec = 70Hz.

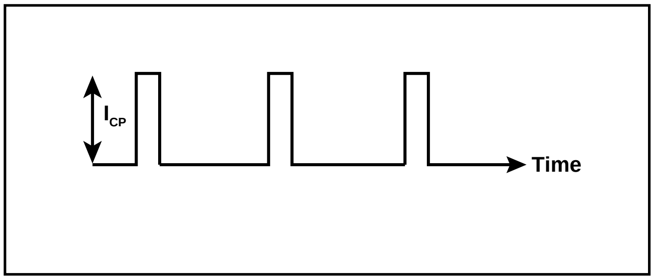


Fig.7 Phase detector current pulses

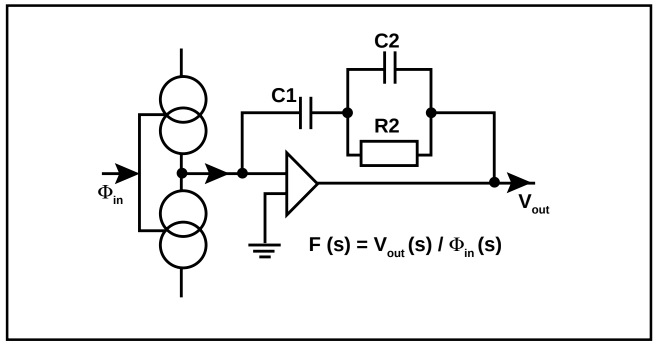


Fig.8 (a) Phase detector and charge pump - third order type 2 loop

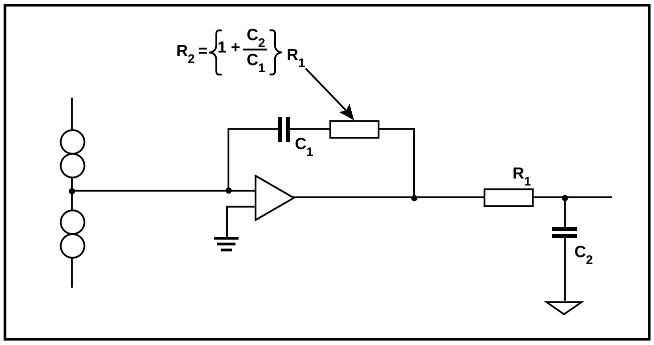


Fig.8 (c) Exact equivalent of Fig.8(a)
(Practical alternative to Fig.8(a))

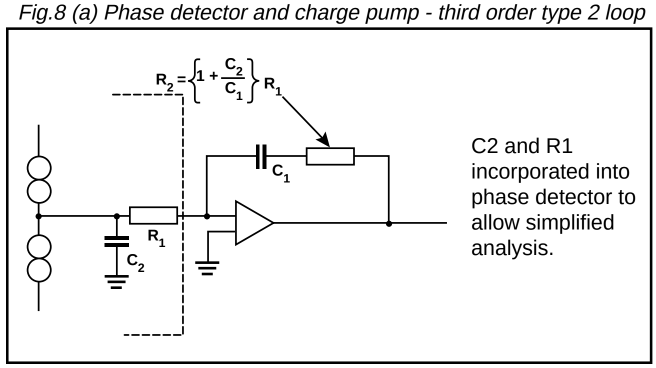


Fig.8 (b) Exact equivalent of Fig.8(a)

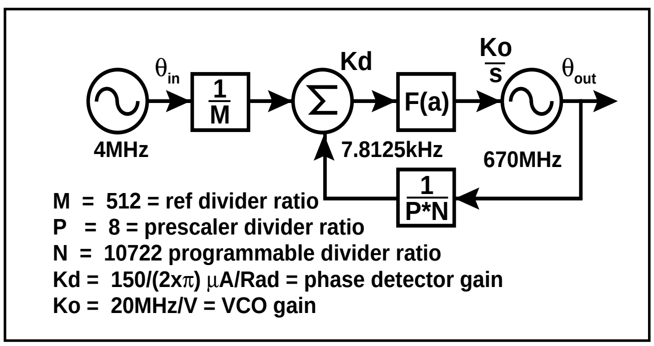


Fig.9 System block diagram

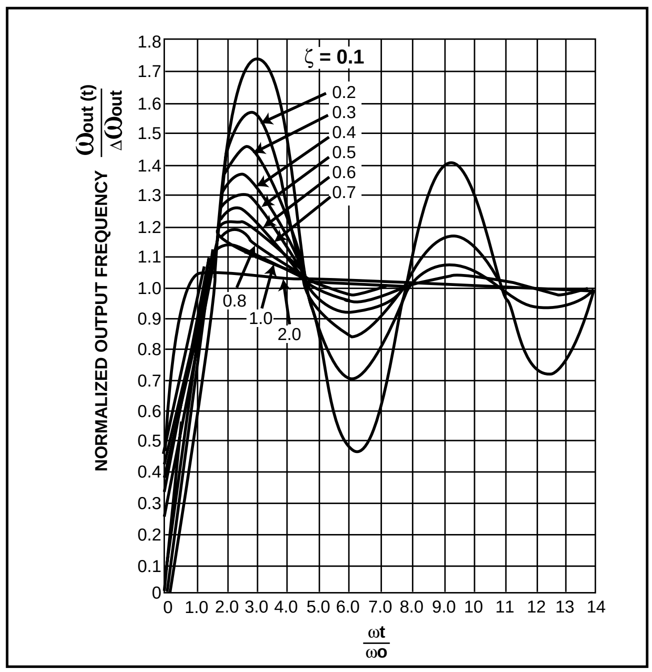


Fig.11 Time domain response to step in frequency

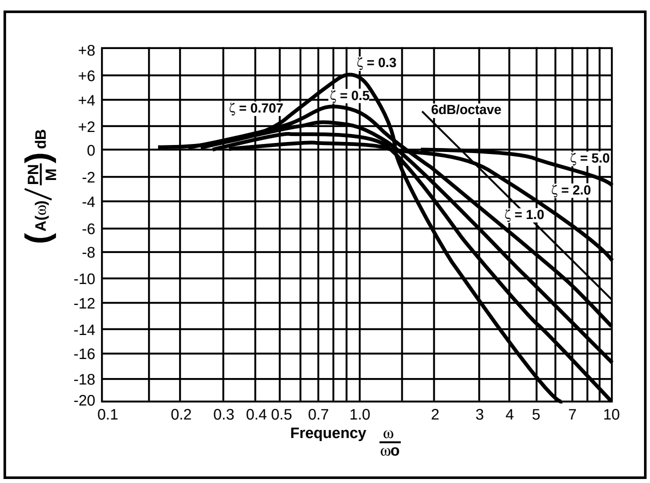
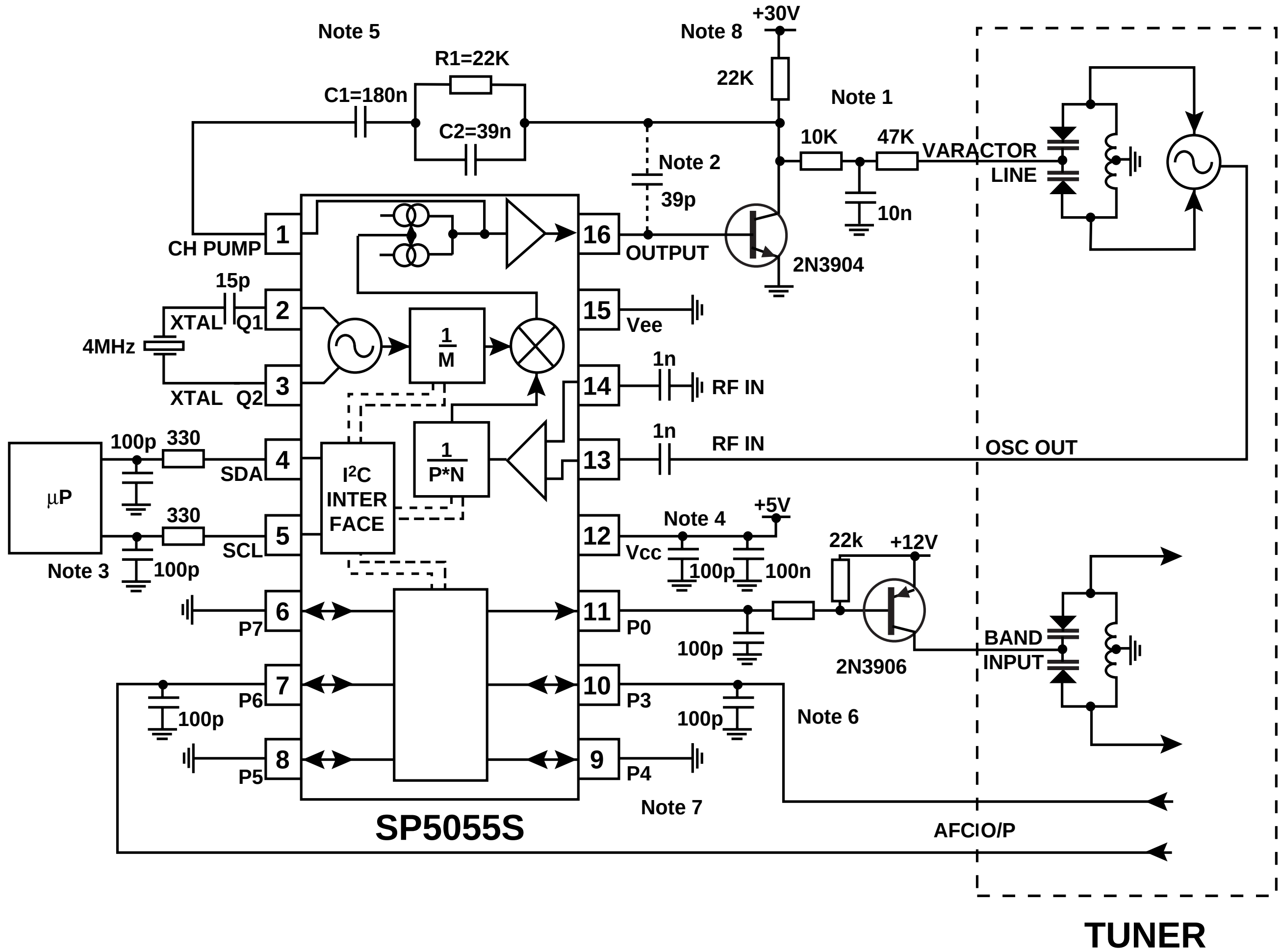


Fig.10 Frequency response of a high gain second order loop



Note 1 : Varactor line filter reduces ripple.
Note 2 : 39pF capacitor reduces radiation into NPN base.
Note 3 : IIC bus filtering reduces transients.
Note 4 : Decouple Vcc rail at both high and low frequencies.
Note 5 : Choose appropriate loop filter components
Note 6 : Decouple unused output ports
Note 7 : Ground unused input ports
Note 8 : When the varactor line disable (OS bit) is set, the 30V supply can be varied to directly control the analog voltage to the varactor.

Fig.6 Typical I²C Synthesiser application

VARACTOR LINE FILTERING

Special care should be taken with the varactor line. A low pass filter may be placed in the varactor line to prevent ripple being fed along the line and mistuning the oscillator. A typical application is shown in Fig.4.

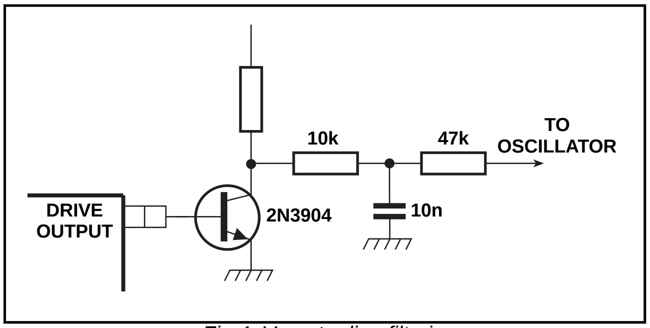


Fig.4 Varactor line filtering

The NPN transistor TR1, connected to the drive output, should be placed as close to the drive output pin as possible. The input to this transistor presents a very high impedance. Any length of track between the drive output of the synthesiser and the base of TR1 can act as an antenna which will feed unwanted signals into the transistor. To minimise this effect, a low value capacitor of, say 39pF may be connected between the base and collector of TR1 (as shown in Fig.5) without modifying the dominant loop characteristics.

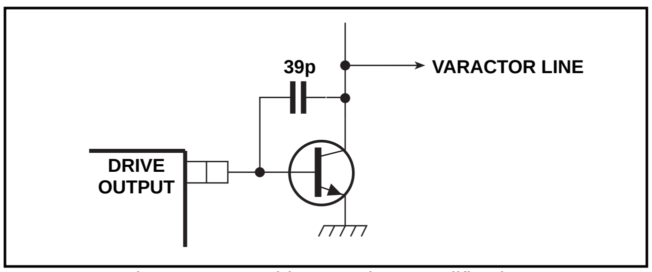


Fig.5 Varactor drive transistor modification

It is important that no other RF signals which may be present in the tuner, for example IF outputs, are routed anywhere near the synthesiser as they can also couple into the device.

All of the above suggestions are made in an attempt to achieve the best possible phase noise and sideband performance for the synthesised oscillator. Whilst a good synthesiser application does not guarantee good phase noise performance, a bad synthesiser application will almost certainly limit the overall performance of the tuner and degrade phase noise compared to that of a free-running oscillator.

CALCULATION OF LOOP COMPONENT VALUES

Applications Circuit (See Figure 6)

A typical synthesiser application circuit is shown in Figure 6. The optional additional filtering (referred to by Note 1 on this diagram) rolls off at a frequency well above the main loop filter. Its main purpose is to reduce any noise picked up on the varactor control line. Consequently its effect is ignored in this analysis. The following is a summary of the derivation of the basic design equations used to calculate the loop filter components.

Phase Detector Gain (See Figure 7)

The phase detector outputs pulses of current I_{CP} µA with a pulse frequency equal to the comparison frequency $\frac{\omega_{in}}{M}$ and width proportional to the phase error. These pulses are averaged by the loop filter so that the phase detector gain is given by:-

$$Kd = \frac{I_{cp}}{2} \ \mu A/\text{radiation} \qquad ....(1)$$

Loop filter analysis (See Figure 8)

The loop filter converts the current pulses from the charge pump into a voltage proportional to the phase error. The filter recommended for normal applications is shown in fig 8(c). The transfer characteristic is :

$$F(S) = \frac{(1+sT_2)}{sT_1\,(1+sT_3)} \qquad \text{where } T_1 = C_1,\; T_2 = (C_1+C_2)\,R_2,\; T_3 = C_2, R_2$$

Procedure for design of filter

Fig.8b shows an exact equivalent of the filter in figure 8(a). It is not possible to implement this configuration since the only points which are accessible are the input and output of the op-amp, but it serves as a useful design model. If C_2 and R_1 are incorporated as a current "pulse integrator" into the phase detector then the remaining components consisting of the op-amp, resistor $[1 + C_2/C_1]\,R_1$ and capacitor C_1 can be regarded as the loop filter.

This procedure allows us to treat the filter as a 2nd order loop rather than the more complex 3rd order loop of figure 8(a). This loop will have a natural frequency of ω_O and damping factor ζ which we can select based on the application. The cut off frequency of the "pulse integrator" would normally be set to $5\omega_O$ or more. By manipulation of the transfer function (see appendix) we can derive simple approximate design formulae for C_1, R_2 and C_2. These are:-

$$C_1 = \frac{KdKo}{PN\omega_O^{\,2}}$$

$$C_2 = C_1/5$$

$$R_2 = \frac{2\,\zeta}{\omega_O\,C_1}$$

Choice of Natural Frequency and Damping Factor

When the synthesiser is reprogrammed, the application will usually require the VCO to settle to the new frequency within a specified time to a specified accuracy. Appendix 3 (Time Domain Response) shows that the time domain response to a frequency step is an exponentially decaying sinusoid. From this the natural frequency ω_O can be calculated if we specify the settling time t_S and the accuracy $\omega_e/\ \omega$, provided we already know the damping factor ζ.

The damping factor must be chosen so that the system remains stable. For this the phase margin should be reasonably high say 0, > 45° or so. See Appendix 3 (Phase margin). The amount of 'overshoot' might also be used to estimate a value for ζ. See Figure 11.

AN168

TV/Satellite Synthesisers - Basic Design Guidelines

Application Note

AN168 - 2.4 June 1995

EXTERNAL NOISE PROBLEMS

I²C BUS RADIATION PROBLEMS

The main problem when designing PCBs using any I²C device is that data and clock are always being transmitted and fed to the transceivers. This can lead to problems with radiation unless suitable precautions are taken.

Coupling from the SCL and SDA lines can often occur where these lines are long tracks leading to the synthesiser. The SCL and SDA lines pose particular problems as clock and data are always present on the I²C databus, regardless of whether the synthesiser is being addressed or not. These can couple into the synthesisier through any of the pins; it is therefore important to ensure that all pins are decoupled where possible. Unused ports should be taken to ground. Small decoupling capacitors may be placed directly on the pin to cut radiation into ports.

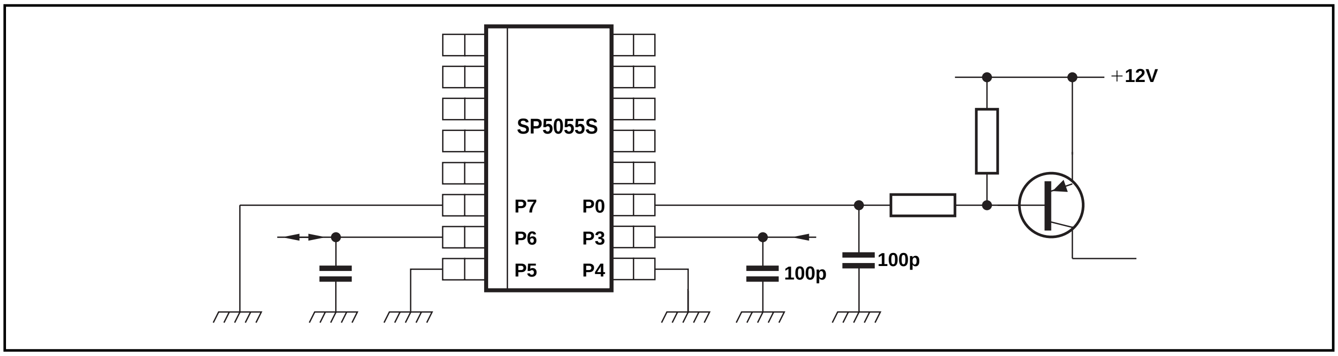


Fig.1 Decoupling/grounding of used and unused ports

I²C BUS LINE FILTERING

I²C bus specifications permit a maximum of 400pF on the SDA andSCL lines. This figure refers to the maximum total capacitance present on the bus so therefore includes other devices. Most applications use a combination of 100pF decoupling capacitors on each line together with a series resistor of up to 100k , depending on the clock rate.

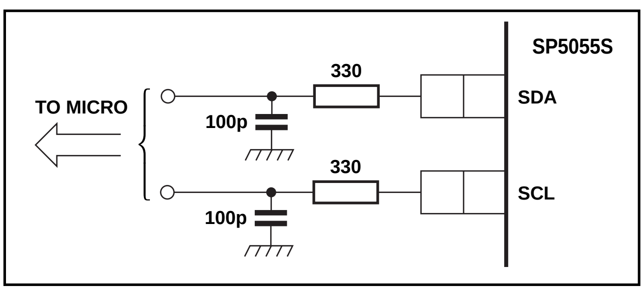


Fig.2 I²C bus line filtering

SYNTHESISER DECOUPLING

Supplies should be decoupled as close to the chip as possible. It is suggested that combination of 100pF and 100nF is used to give the best possible immunity against low and high frequency noise.

Layout

Care must be taken with layout to ensure that the supply rails are as short as possible and that no loops (either ground or supply) exist. If the layout permits, the V_{CC} line should not be routed near the loop filter.

Grounding

The synthesiser should be taken to a clean ground separate from the track used to ground any of the oscillators. If possible, shielding should be introduced between the oscillators and the synthesiser to ensure that no spurious coupling occurs.

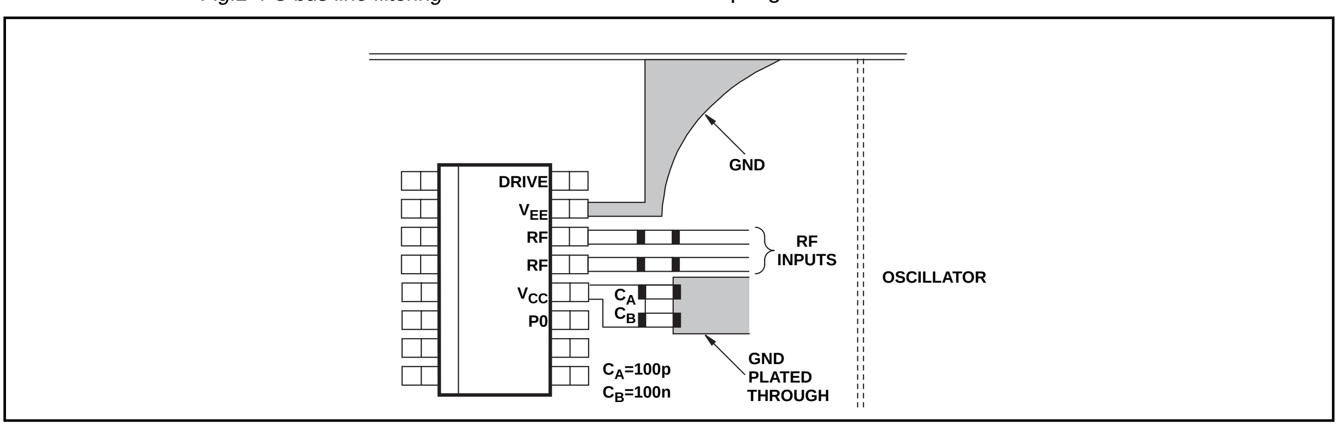


Fig.3 Layout and decoupling of synthesiser supply pins